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WILLIAM E. LEWIS
RYAN, MASON & LEWIS, LLP
90 FOREST AVENUE
LOCUST VALLEY, NY 11560

EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/682,520
Filing Date: September 13, 2001
Appellant(s): O'DOWD, ANTHONY JOHN

William E. Lewis
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed October 7, 2005 appealing from the Office action mailed January 4, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The Examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The Appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The Appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

Claims 1, 13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 6,173,395 to Wisor et al. (hereinafter "Wisor").

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wisor.

Claims 4-12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wisor in view of U.S. Patent 6,353,924 to Ayers et al. (hereinafter "Ayers").

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,173,395	Wisor et al.	01-2001
6,353,924	Ayers et al.	03-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 6,173,395 to Wisor et al. (hereinafter "Wisor").

Regarding claim 1:

Wisor discloses:

- a method for tracing the execution path of a computer program comprising at least one module including a plurality of instructions ("to enable the user to trace the sequence of execution of instructions..." in col. 3 lines 1-2)
- at least one of said instructions being a branch instruction ("The stored data identifies whether or not certain branches in the test program were taken..." in col. 4 lines 58-59)
- identifying each branch instruction ("involves detecting the branch instructions..." in col. 6 lines 16-17)
- evaluating each branch instruction to be one of true and false, and responsive to an evaluation of true, pushing a unique identifier into a predefined area of storage, wherein said unique identifier is associated with the instructions executed as a result of said evaluation of true ("When a test program is executed, a trace record is generated and stored in the BTHB (branch trace history buffer)...the bitmap entries are generated for a series of conditional branches and contain individual bits which represent the taken or not-taken status of the branches" in col. 3 lines 11-21. Further, "1's represent taken branches and 0's represent not-taken branches." in col. 7 lines 47-48. Note Figure 3 and the corresponding sections of the disclosure, of which depicts one exemplary bitmap generated as a result of tracing, and is representative of one BTHB entry. Each 1 and 0 is uniquely assigned a bit position in the bitmap entry in the order that the branch is encountered within the program and is furthermore uniquely associated to the specific taken/not-taken branch. Finally, the conditional of taken/not-taken represents a true/false conditional.)

substantially as claimed.

Regarding claim 13 and 14:

Claims 13 and 14 are directed a an apparatus and method for performing the method of claim 1, and are rejected for the reasons set forth in connection with claim 1.

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,173,395 to Wisor et al, hereafter referred to as Wisor.

Regarding claim 2:

The rejection of claim 1 is incorporated, and further, Wisor discloses providing the predefined area of storage with memory (Note Figure 1, item 30). Wisor does not explicitly disclose the memory as being volatile memory. Official Notice is taken that at the time the invention was made, the use of volatile memory was well known to one of ordinary skill in the art. As such, one of ordinary skill in the art at the time the invention was made would choose to utilize volatile memory for the system disclosed by Wisor for the purposes of freeing memory space when the computer is powered down and no longer in use.

Regarding claim 3:

The rejection of claim 1 is incorporated, and further, Wisor discloses providing the predefined area of storage with memory (Note Figure 1, item 30). Wisor does not explicitly disclose the memory as being non-volatile memory. Official Notice is taken that at the time the invention was made, the use of non-volatile memory was well known to one of ordinary skill in the art. As such, one of ordinary skill in the art at the time the invention was made would choose to utilize non-volatile memory for the system disclosed by Wisor for the purposes of retaining information in memory when the computer is powered down and no longer in use.

Claims 4-12 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,173,395 to Wisor et al, hereafter referred to as Wisor in view of U.S. Patent 6,353,924 to Ayers et al, hereafter referred to as Ayers.

Regarding claim 4:

The rejection of claim 1 is incorporated, and further, Wisor discloses outputting the contents of the storage area at a predetermined point in time ("the contents of the BTHB and the test code are retrieved into the test station" in col. 3 lines 22-24). Wisor does not explicitly disclose outputting the contents to a file. Ayers discloses in an analogous trace recording system outputting trace sequence information to a file as claimed ("The sequence information can be recorded...to a disk file" in col. 3 lines 60-61). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the file saving capabilities of Ayers with the trace recording system of Wisor, as this would enable a user to archive tracing records in the system disclosed by Wisor.

Regarding claim 5:

The rejection of claim 4 is incorporated, and further, Wisor discloses outputting the trace information upon exit from at least one module as claimed ("After a program is executed on the system under test, the contents of the BTHB are retrieved into the computer system" in col. 9 lines 11-12)

Regarding claim 6:

The rejection of claim 5 is incorporated, and further, Wisor discloses outputting the contents of the storage area at the same time as the exit trace information as claimed ("After a program is executed on the system under test, the contents of the BTHB are retrieved into the computer system" in col. 9 lines 11-12)

Regarding claim 7:

The rejection of claim 4 is incorporated, and further, Wisor discloses determining whether the storage area is full, and responsive to a positive determination, outputting the contents as claimed ("Tracing can be set to stop...when the BTHB is full" in col. 8 lines 34-35)

Regarding claim 8:

The rejection of claim 4 is incorporated, and further, Wisor does not explicitly disclose determining whether a failure has occurred within the program, and responsive to a positive determination, outputting the contents to a file. Ayers discloses in an analogous trace recording system determining whether a failure has occurred and outputting the contents to a file as claimed ("upon some triggering event such as a system crash, the post-processor writes out the sequence record..." in col. 9 lines 65-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the failure-responsive outputting capabilities of Ayers with the trace recording system of Wisor, as this would enable a user to obtain the exact sequence of instructions that executed prior to a crash in the system disclosed by Wisor as stated in col. 2 lines 21-27 of Ayers.

Regarding claim 9:

The rejection of claim 4 is incorporated, and further, Wisor discloses determining whether the predefined area of storage is full, and overwriting the first unique identifier in the storage area as claimed ("The buffer can be set to wrap around so that the oldest entries are overwritten by the newest entries..." in col. 8 lines 35-37)

Regarding claim 10:

The rejection of claim 9 is incorporated, and further, Wisor discloses writing the position of the most recent unique identifier to be written out to the storage area to the storage area as claimed ("When a conditional branch is found, a counter is incremented..." in col. 9 lines 57-58. The counter represents the position.)

Regarding claim 11:

The rejection of claim 10 is incorporated, and further, Wisor discloses using the position to determine number of unique identifiers that have been overwritten as claimed ("the BTHB contents are checked to determine whether the number of bits...matches the corresponding number of conditional branches in the instruction sequence" in col. 9 lines 18-21)

Regarding claim 12:

The rejection of claim 11 is incorporated, and further, Wisor does not explicitly disclose increasing the size of the predefined area of storage. Ayers discloses in an analogous trace recording system increasing the size of the predefined area of storage as claimed ("The buffer size limits the amount of traceback history...Preferably this limit can be set dynamically..." in col. 6 lines 26-28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the

size-increasing capabilities of Ayers with the trace recording system of Wisor, as this would enable a user to obtain a larger amount of traceback history in the system disclosed by Wisor.

Regarding claim 15:

Claim 15 recites a compiler for performing the method of claim 1, and is rejected for the reasons set forth in connection with claim 1. For the added limitation of a compiler, Wisor does not explicitly disclose a compiler. Ayers discloses in an analogous trace recording system a compiler for instrumenting a computer program as claimed (Note Figure 4, items 311 and 313 and the corresponding sections of the disclosure). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a compiler in the system of Wisor, as this would enable source code to be executed and subsequently traced.

(10) Response to Argument

1. Rejection of claims 1, 13 and 14 under 35 U.S.C. § 102(e)

Starting at paragraph two, page 5 of the brief, Appellant states:

> Wisor does not disclose pushing a unique identifier into a predefined area of storage, wherein said unique identifier is associated with the instructions executed as a result of said evaluation of true," as recited in claim 1; "a pusher, responsive to an evaluation of true, for pushing a unique identifier into a predefined area of storage, wherein said unique identifier is associated with the instructions executed as a result of said evaluation of true," as recited in claim 13; or "instrumenting said instructions associated with an evaluation of true with a signature instruction, wherein said signature instruction causes a unique identifier to be pushed into a predefined area of storage upon execution of said true instructions at run-time," as recited in claim 14.

Substantially similar arguments have been presented since Appellant's first response dated August 19, 2004, the main point of contention being whether or not Wisor discloses "pushing a unique identifier...as a result of said evaluation of true" as required by the claims.

The Examiner has cited in the past the ability of Wisor to trace branch history through the use of a branch trace history buffer ("BTHB"), specifically noting column 3, lines 11-21 of Wisor which state:

> When a test program is executed, a trace record is generated and stored in the BTHB (branch trace history buffer)...the bitmap entries are generated for a series of conditional branches and contain individual bits which represent the taken or not-taken status of the branches.

The Examiner has interpreted the ability of Wisor to populate a BTHB with individual bits representing the taken or not-taken status of branches to equate to the required limitation of "pushing a unique identifier into a predefined area of storage...as a result of said evaluation of true." In response, Appellant has argued, "such bitmap entries are expressly described as containing 'individual bits which represent the taken or not-taken status of the branches.' Thus, there is nothing unique about the bits since they merely represent whether a branch is taken or not taken." Appellant further argues on page 7 of the brief, "it is clear that two bitmap entries referring to 'taken' conditional branches in Wisor may be the same and, therefore, not unique since both conditional branches would have the same bit set to a logic one to indicate it is a conditional branch that is 'taken' (as opposed to 'not taken')..."

The Examiner respectfully disagrees with this argument. In review, Wisor discloses enabling a user to trace the sequence of execution of instructions in test code. Entries corresponding to the execution of control instructions and other significant trace events are stored in a BTHB. (column 2, line 67 to column 3, line 3). Further, as noted in column 7, lines 2-4, Wisor discloses "a series of

consecutive conditional branches is represented as a series of consecutive bits in a single entry in the BTHB." Furthermore, the BTHB consists of a number of bitmap entries, one exemplary bitmap being shown in Figure 3. Column 7, lines 42-48 state, "FIG. 3 shows an example of a bitmap...In this example, 1's represent taken branches and 0's represent not-taken branches." Accordingly, the system disclosed by Wisor must make a determination as to whether a branch was taken or not-taken, effectively evaluating a true or false concerning whether branches were taken. Furthermore, as noted above, either a 1 or a 0 is inserted into the bitmap as a result of the evaluation. Accordingly, Wisor initially discloses that, responsive to an evaluation of true (branch taken or not-taken), pushing an identifier into a predefined area of storage (inserting either a 1 or a 0 into the bitmap stored in the BTHB), wherein the identifier is associated with the instructions executed as a result of said evaluation of true (1's represent taken branches and 0's represent not-taken branches). The question then become whether the individual 1's and 0's inserted into the bitmap entry of Wisor constitute "unique" identifiers as required by the claims.

As noted above, Appellant argues that they are not unique in that two entries in the bitmap corresponding to taken branches would have bit set to logic one to indicate that the conditional branch has been taken. As an example, note Figure 3, bit positions 26 and 27, wherein a bitmap entry is shown having bit positions 26 and 27 each with logic one indicating that a branch was taken. Appellant argues that because both bit positions contain a "1" they do not constitute unique identifiers inserted into the bitmap. However, it is the Examiner's position that there are at least two reasonable interpretations as to why these constitute unique identifiers.

1. The individual 1 and 0 bits inserted into the bitmap entries are unique in that each 1 or 0 inserted into a specific bitmap entry in the BTHB is assigned a specific bit position in

the bitmap entry. Referring again to Figure 3, by this interpretation, the "1" inserted into bit position 26 is unique from other "1's" in that it is the only "1" inserted into bit position 26 of that specific bitmap entry in the BTHB.

2. The individual 1 and 0 bits inserted into the bitmap entries are unique in that each 1 or 0 inserted into a specific bitmap entry in the BTHB (i.e. in the order that the branches are encountered in the program) is uniquely associated with the specific conditional branch it represents. Referring again to Figure 3, by this interpretation, the "1" inserted into bit position 26 is unique from other "1's" in that it is the only "1" which corresponds to the specific branch that was taken at the time of the evaluation, and bit position 27 would represent a completely different branch from bit position 26.

The Examiner alluded to this interpretation in the Advisory Action, to which Appellant argued on page 9 of the brief, "Whether or not this is true, the value (identifier) that is stored in accordance with the entry is not unique..." However, the Examiner considers these arguments to not be fully commensurate with the scope of the claims. While it may be true that the individual identifiers themselves are not unique, the claims as written do not specify how the identifiers are to be unique (emphasis added), only that they are unique according to some reasonable interpretation. A "1" identifier may not necessarily be unique from another "1" identifier unless the identifier is, through some other means, unique, whether it is uniquely associated with a specific branch or instruction (emphasis added), or whether it is uniquely assigned to a specific bit position (emphasis added). Accordingly, the Examiner contends that Wisor discloses the required limitations.

2. Rejection of claims 2 and 3 under 35 U.S.C. § 103(a)

Appellant's arguments on page 9 of the brief concerning the rejection of claims 2 and 3 under 35 U.S.C § 103(a) rely on arguments concerning the deficiency of anticipation under 35 U.S.C. § 102(e), of which have been addressed above, and are consequently not addressed here.

3. Rejection of claims 4-12 and 15 under 35 U.S.C. § 103(a)

Appellant's arguments on pp. 9 and 10 of the brief concerning the rejection of claims 4-12 and 15 rely on arguments concerning the deficiency of anticipation under 35 U.S.C. § 102(e), of which have been addressed above. Additionally, Appellant argues that the prior Office Actions fail to address the distinction of a "file" as required by claim 4. In response, it is noted that the final Office Action presented a combination of Wisor and Ayers showing that it would have been obvious to one or ordinary skill in the art at the time the invention was made to utilize a disclosed ability of Ayers to record to a disk file (note column 3, lines 60-61 of Ayers) with the tracing system of Wisor. Furthermore, Appellant has not argued why it would not have been obvious to one of ordinary skill in the art to combine the teaching of Wisor and Ayers, subsequently, the rejection is considered proper.

Finally, with reference to claims 5-8 and 9-12, Appellant presents general allegations of patentability without specifically showing how the cited portions of Wisor and Ayers do not read on the limitations of the claims, instead stating that "these features in Wisor and Ayers are not the same as the features recited in claims 9-12." (page 10 of the brief). Accordingly, the Examiner considers the rejection proper.

(11) Evidence Appendix and Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the Examiner in the Related Appeals and Interferences section of this Examiner's answer. Furthermore, as Appellant did not include an Evidence Appendix and Related Proceeding(s) Appendix in the brief, it is assumed that the Appellant meant to include both appendixes with a statement of "NONE."

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Trenton J. Roche

April 25, 2006

Conferees:

Kakali Chaki

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

TUAN DAM
SUPERVISORY PATENT EXAMINER

Tuan Dam